

Lesson Plan

Name of the Faculty : MR. SAHARSH GERA (THEORY)
 Discipline : Electrical & Electronics Engineering
 Semester : 6th
 Subject : Computer Organization & Architecture (PEC-EEE-12G)
 Lesson Plan Duration : 15 Weeks (from MAY, 2021 to AUG, 2021)

**** Work Load (Lecture/ Practical) per week (in hours): Lecture-03**

Week	Theory	
	Lecture day	Topic(Including assignment/test)
1 st	1 st	Data representation: Data Types
	2 nd	Complements
	3 rd	Fixed-Point Representation, Conversion of Fractions
2 nd	1 st	Floating-Point Representation
	2 nd	Gray codes
	3 rd	Decimal codes, Alphanumeric codes
3 rd	1 st	Error Detection Codes
	2 nd	Register Transfer and Microoperations : Register Transfer Language
	3 rd	Register Transfer, Bus and Memory Transfers
4 th	1 st	Arithmetic Microoperations
	2 nd	Logic Microoperations
	3 rd	Shift Microoperations, Arithmetic Logic Shift Unit (ASSIGNMENT – 01)
5 th	1 st	Basic Computer Organization and Design : Instruction Codes
	2 nd	Computer Registers
	3 rd	Computer Instructions, Timing and Control

6 th	1 st	Instruction Cycle
	2 nd	Memory-Reference Instruction
	3 rd	Input-Output Instruction, Complete Computer Description
7 th	1 st	Design of Basic Computer
	2 nd	Design of Accumulator Logic
	3 rd	Central Processing Unit : General Register Organization, Stack organization
8 th	1 st	Instruction Format
	2 nd	Addressing Modes
	3 rd	Data Transfer and Manipulation, Program Control
9 th	1 st	RISC
	2 nd	CISC (ASSIGNMENT – 02)
	3 rd	Pipelining: Basic Concepts of Pipelining, Throughput and Speedup
10 th	1 st	Pipeline Hazards
	2 nd	Parallel Processors: Introduction to Parallel Processors
	3 rd	Concurrent access to memory and Cache Coherency (ASSIGNMENT – 03)
11 th	1 st	Input-output Organization : I/O device interface , I/O transfers–program controlled
	2 nd	interrupt driven and DMA
	3 rd	Privileged and Non-Privileged Instructions, Software Interrupts
12 th	1 st	Memory organization: Memory Hierarchy
	2 nd	Main Memory
	3 rd	Auxiliary Memory, Associative Memory
13 th	1 st	Cache Memory
	2 nd	Associative Mapping
	3 rd	Direct Mapping, Set-Associative Mapping
14 th	1 st	Writing into Cache
	2 nd	Cache Initialization, Virtual Memory.
	3 rd	(ASSIGNMENT – 04), Revision of unit-01
15 th	1 st	Revision of unit-02
	2 nd	Revision of unit-03



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	3 rd	Revision of unit-04
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